The ForteMedia FM801-AU is designed to suit the most cost-effective, practical, PCI Audio solution for both desktop computer and notebook computer. It integrates the essential features of today's gaming requirements without compromising the PC98 criterion for audio quality. FM801-AU integrates the PCI 2.2 bus master controller, music synthesis, SoundBlaster Pro Engine, sampling rate converter, digital mixer, CODEC interface, game ports, I2S ports and S/PDIF port. The FM801 solution leverages its simple but effective hardware/software architecture and the uprising HSP (host-based signal processing) support on Direct Sound, WaveTable and Direct 3D positional audio, and is therefore the most practical PCI audio solution. The CODEC interface is fully compliant to AC-97 ver.2.1 and is capable of supporting multiple speakers for either docking application or merely a PC theater set up for gaming and audio enjoyment. With its 3.3 volts operating voltage, ACPI power management, PME and PCI clock-run supports, plus a small 100-pin PQFP package size, the FM801 surely is the right choice for today's PCI audio solution.

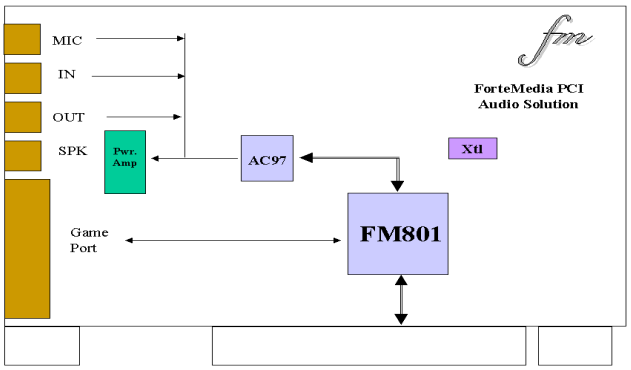
Audio Features

- Proprietary Logic for Real DOS SoundBlaster Pro games support
- Hardware Synthesizer for AdLib and General MIDI compatibility
- Optional QSound HSP dynamic 3-D positional audio support
- Variable Rate SRC(sampling rate converter) support
- AC-97 2.1 compliance
- Multiple speakers, 2/4/6 channels support
- Hardware push button volume control (up/down/mute)
- Dual game ports support; MPU-401 and I2S port
- S/PDIF Digital input
- S/PDIF AC-3 raw data output support
- 18 bits Audio CODEC support

PCI and Others

- 3.3 V operating voltage with 5V tolerance
- PCI v.2.2 compliance with bus master and scatter-and-gather capability
- Proprietary Legacy mode, DDMA, Serial IRQ, and PC/PCI support
- Four GPIO (General Purpose I/O) pins
- ACPI and PCI CLKRUN power management
- DOS,Win95,98,NT,WDM,Linux,OSS drivers
- 100 pin PQFP package, 14 x 14 x 1.4 mm

FM801 Typical Add-On Card Application

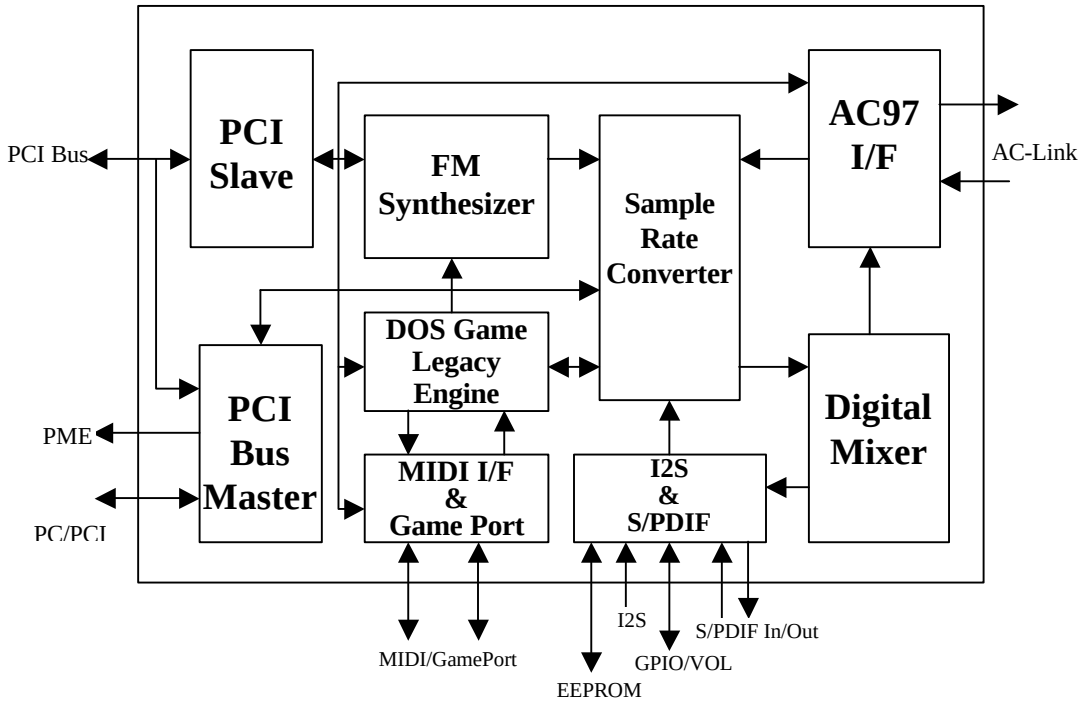


Architecture

FM801-AU is a cost effective, highly integrated PCI audio controller for today's high performance multimedia PC audio requirements. Based on ForteMedia's own proprietary DOS game interface, hardware MIDI synthesis engine and high bandwidth PCI interface, FM801-AU supports games under both Microsoft Windows and DOS environments without compatibility issues. With its low cost structure and support high sound quality AC97 architecture along with the assured game compatibility, the FM801-AU is the desired PCI audio solution. FM801-AU can be physically partitioned into the following functional blocks:

- PCI Interface
- FM synthesizer
- Legacy DOS Game Engine, MIDI Port and Game Port
- Peripheral Interfaces (I^2S, VOL, GPIOs and SPDIF, EEPROM)
- AC97 CODEC Interface, SRC and Digital Mixing

FM801-AU Block Diagram



PCI Interface

The PCI Interface is designed per specification of PCI rev.2.2 with scatter and gather capability, it provides the interface to the 33MHz, 32-bit PCI bus with the ability to support PCI configuration (PCI Plug & Play), PCI slave I/O cycles and PCI bus master memory read/write cycles. It interfaces to all the internal blocks, serving as the gate to the system. This block can be further partitioned into 3 sub-blocks, DMA Controller, PCI slave IF and PCI master IF. PCI slave IF handles the PCI configuration and also translates the PCI I/O cycles to internal I/O cycles. Moreover, this sub-block is also the center of power controlling to the whole chip. PCI master IF mainly interfaces to the Streaming Engine and internal DMAC, providing the scheme of system memory access or DMA emulation to the SB Engine. It contains 2 sets of Ping-Pong buffer(16bytesX2) for playback and capture. DMA Controller will provide the functionality of ISA DMA Controller, thus resolving the legacy Audio issues on PCI bus. It also provides the address when PCI bus master is activated. It also provides the Plug-and-Play (PnP) compatibility with the Intel/Microsoft PnP specification. It support PCI interrupts and DMA channels, and allows the PC to automatically configure it into the system upon power up

PC/PCI

PC/PCI is a mechanism that was defined and developed by Intel's Mobile/Handheld Products Group (MHPG) as a mobile docking solution which allows ISA slots to exist in docking stations connected to the notebook's PCI bus. This scheme is now being applied to the desktop PC as well. By providing a new arbitration construct, consisting of a serialization protocol for encoding and decoding DMA requests/grants, a request/grant pair, distinct from the PCI bus pair, is used to bundle requests for any combination of 8237 supported DMA channel(s) for each device needing DMA support. This encoded mapping on the PC/PCI agent's request/grant pair provides the pathway that enables a PCI resident agent to deliver 8237 style DMA requests to the system without requiring separate and distinct DREQ/DACK# pins for each DMA channel that is used by the PC/PCI agent.
Intel LX chipsets are currently support PC/PCI functionality .

FM Synthesizer

This is a 20-voice, 4-operator music synthesis. This block interfaces to the PCI slave block, allowing the host system to control the synthesis parameters via I/O access.

Legacy DOS Game Engine, MIDI Port and Game Port

This section includes 3 sub-blocks: SB-Pro compatible state machine, bi-directional MPU-401/MIDI port and Game port.

Legacy DOS Game Engine

It interfaces to the PCI for Real DOS Game legacy I/O port access and DMA emulation. It supports DDMA, “Serial-IRQ”, PC/PCI and ForteMedia’s own proprietary modes.

MIDI Port

A bi-directional MIDI interface is provided to allow connection of external MIDI devices. The MIDI interface includes 16-byte FIFOs for the MIDI TX and RX paths.

Game Port

The FM801-AU game port interface is designed to work in two modes: 1) hardware polling digital mode and 2) analog mode. The game port control signals include four button signals and four position signals. For both modes, the processing of the button signals are the same. They are not latch, but the switch states are just passed to the data bus when they are required. The position signals are handled differently, depending upon the mode being used.

Peripheral Interfaces

Peripheral Interface includes all the miscellaneous input and output interfaces: AC97 Codec IF, I^2S input ports for ZV audio application and one S/PDIF output port.

I2S (Enhanced)

The **I2S** interface which is designed for the purpose of interconnecting consumer and professional digital audio products with very low Jitter clock recovery for precise digital to analog conversion.

S/PDIF Digital Input

The FM801-AU utilized the digital audio interface S/PDIF bi-phase-mark encoding to reduce cross-talk from the data portion of the clock. The FM801-AU device can auto detect if there is the S/PDIF input connection is ON or OFF. It also can distinguish if an input stream is an audio PCM stream or an AC-3 raw data stream. When detecting an audio PCM stream, FM801-AU can accept the following sampling rate: 32KHz, or 44.1 KHz, or 48KHz.

S/PDIF AC-3 Raw Data Output Support

The FM801-AU can support S/PDIF output in both audio PCM format or as an AC-3 raw data format. The output audio stream can be formatted as a 16-bit audio stream with the sampling rate of 48KHz.

Shared I/O Interfaces

In order to maintain the minimum pin count to 100, few functional pins are shared and multiplexed internally. They are the hardware volume control pins, GPI/O pins and EEPROM pins. They are shared with SPDIF, AC97, PCLKRUN pins or among themselves.

GPI/O and Volume Control

Four GPI/O multiplexed with volume control pins can be exercised on FM801-AU. GPIO[3:1] are multiplex pins shared with volume control and EEPROM. The definition is as following:

GPIO[3]/Volume Mute/EEPROM(93c57) Data Out
GPIO[2]/Volume Down/EPROM(93c57) Data In
GPIO[1]/Volume Up/EPROM Serial Clock

for general purpose I/O pin use -- FM801-AU output pin, you can control/program on board other device logic action. E.g. AM/FM radio chip or as input pin for Host polling status of signals.

for volume control purpose -- the Volume Control can offer user direct control master volume output over a range of 46.5 dB in 32 steps with most convenience.

Volume Down: support discrete push or continuous push.

Volume Up: support discrete push or continuous push.
Mute: supports discrete push only, repeat push will trigger mute to unmute

EEPROM

Three types are supported, 93C57, 24C00 and 24C01, the selection is through the pin# 86 and pin# 90

AC97 Interface, SRC and Digital Mixing

The FM801-AU supports the AC-Link, which is defined in the Audio Codec'97 Component Specification, as a peer-to-peer communications link between a digital audio controller and an Audio Codec. The FM801-AU functions as the "AC'97 Digital Controller referred to in the Audio Codec'97 Component Specification. FM801-AU also provide SRC and Digital Mixing for FM Midi, Wave, Sound Blaster, I2S, S/PDIF and AC97 audio streams.

AC97 Interface

The FM801-AU AC97 interface compliant with the rev. 2.1 specification, and support one master CODEC and one slave CODEC.

FM801-AU CONNECTION TO THE AC'97 CODEC

The FM801-AU communicates with the AC'97 via a digital serial link called AC-Link. AC-:Link is a 5-pin, bi-directional, fixed data rate, serial, PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses to the AC'97 Codec device employing a time division multiplexed (TDM) scheme. For details of AC97 CODEC, please refer to individual CODEC manufacture's IC specification.

FM801-AU Signal Name	FM801-AU I/O Type	AC'97 Signal Name	AC97 I/O Type	Description
AC97_RST	O	RESET#	I	Master H/W Reset AC'97 Codec from FM801-AU
AC97_FS	O	SYNC	I	48-Khz fixed rate frame sync from FM801-AU
AC97_SDI	I	SDATA_IN	O	Serial, time div/multiplex in stream to FM801-AU
AC97_SDO	O	SDATA_OUT	I	Serial, time div/multiplex out stream from FM801-AU
AC97_SCLK	I	BIT_CLK	O	12.288-Mhz serial data clock

AC97 control register access

1. Host can access the Codec index registers through FM801-AU control register (0x2A~2D). For register write, Host has to poll bit-9 of Codec Command Port (0x2A~2B) first until it's ready. After making sure that Hw is ready to access Codec registers, host can program the data port (0x2C~2D) first, then it should issue 'write command' and the index address to register 0x2A to trigger the Hw to start programming Codec.
2. For register read from Codec, Host has to poll bit-9 of Codec Command Port (0x2A~2B) first until it's ready. Host is then allowed to issue the 'read command'

and the address to register 0x2A . To read the data, Host starts polling bit-8 of it until it is set, then it can read the data from data port at 0x2C~2D.

Resetting the AC'97 CODEC

The AC'97 Codec Specification provides for three types of AC'97 Codec reset:

1. Cold AC'97 Reset, where all AC'97 Codec logic is initialized to its default state
2. Warm AC'97 Reset, where the contents of the AC'97 Codec register set are left unaltered
3. Register Reset, which only initializes the AC'97 Codec registers to their default states

AC-Link Low Power Mode

The AC-Link signals can be placed in a low-power mode. When the AC'97 Codec General Purpose register is programmed to the appropriate value, both AC-Link signals, (BIT_CLK) and (SDATA_IN) will be brought to and held at a logic low-voltage level (BIT_CLK) and (SDATA_IN) from the AC'97 Codec to the FM801-AU are transitioned low immediately following the decode of the write to the General Purpose register. When the FM801-AU driver is ready to program the AC-Link into its low-power mode, slots 1 and 2 are the only valid stream in the audio output frame. At this point in time it is assumed that all sources of audio input have also been neutralized. The FM801-AU driver should also drive the FM801-AU AC-Link signals, (AC97_FS), and (AC97_SDO), low after programming AC'97 to this low power, "halted" mode.

Waking Up AC-Link

Once the AC'97 Codec has been instructed to halt AC97_SCLK, a special "Wake Up" protocol must be used to bring the AC-Link to the active mode since normal audio output and input frames cannot be communicates in the absence of AC97_SCLK. There are two methods for bringing the AC-Link out of a low power, halted mode: Cold AC'97 Reset and Warm AC'97 Reset. The current Power Down State would ultimately dictate which form of AC'97 reset is appropriate. Regardless of the method used, the FM801-AU will perform the Wake -up task.

Once powered down, re-activation of the AC-Link via re-assertion of the (AC97_FS) signal (Warm AC'97 Reset method) must not occur for a minimum of four audio frame times following the frame in which the Power Down was triggered. When AC-Link powers up it indicates readiness via the Codec ready bit (input slot 0, bit 15).

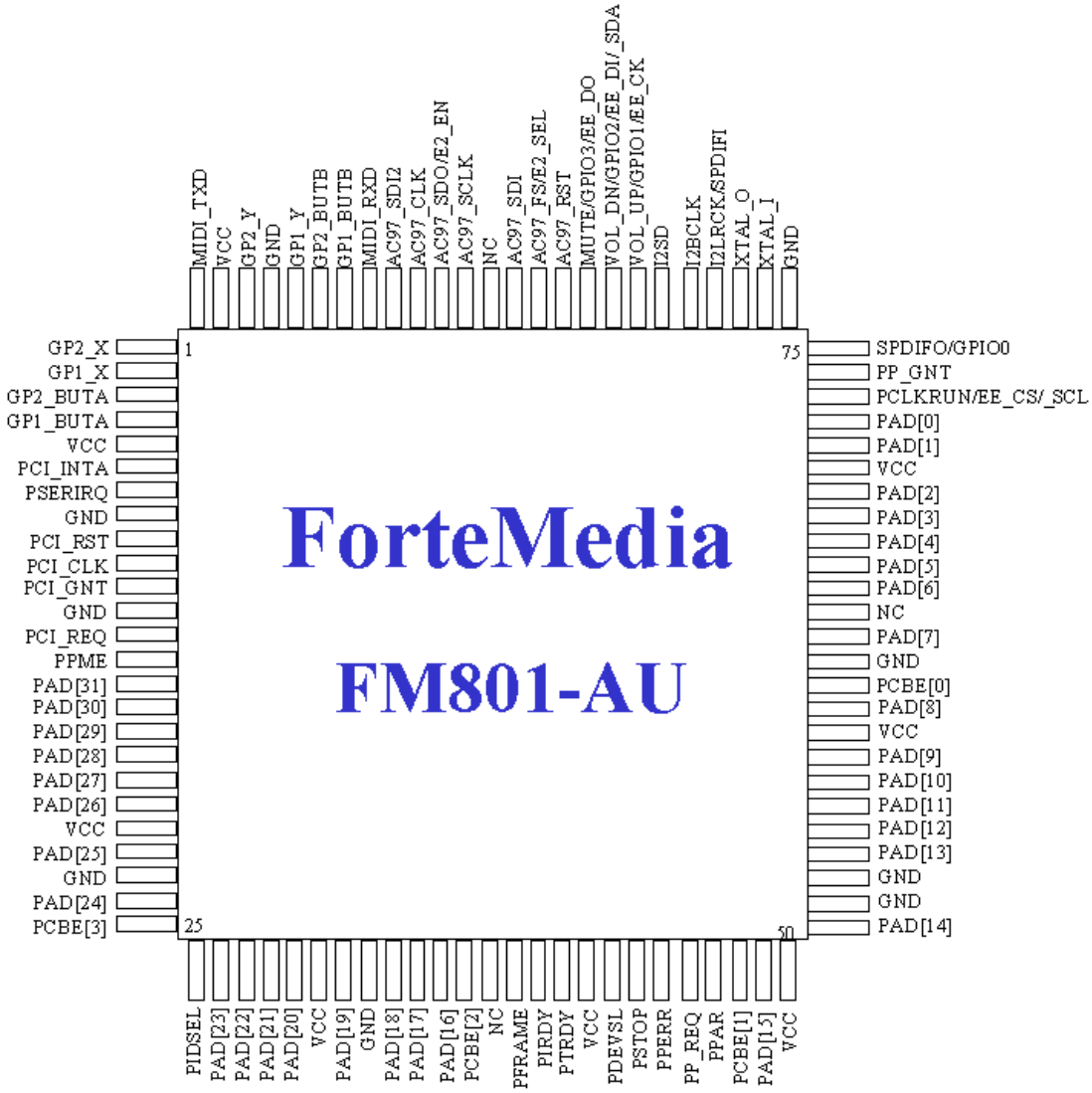
SRC and Digital Mixing

Streaming Engine includes 3 main sub-blocks: Data Flow Controller, Sample Rate Converter and Digital Mixer. FM801-AU supports variable sampling rate AC 97 CODEC. Three sampling rates are supported, 48KHz, 44.1KHz, and 32KHz. Sample Rate Converter will read the data from each sound source (FM, PCM Data, I2S) and converted it to 48khz data streams. Digital Mixer will then mix these sound sources into one output stream @48Khz and send it to Codec IF and SPDIF. For Capture, SRC will read the recording data either from Codec IF, FM or I2S. After converting the data stream from 48Khz to the designate sample rate, SRC will write the recording data into PCI Capture FIFO. PCI master will then execute bus master to write the data back to the system memory when one of the Ping-Pong FIFO is filled. Data Flow Controller will convert and pack the data into the desired format. For playback, it will throw away the junk and data and convert the non-16 bit PCM data into one uniform format: 16-bit stereo signed data for SRC to process. For

capture, DFC will convert the 16-bit signed data into the desired format(8-bit/16-bit, Mono/Stereo) and pack into right alignment. Peripheral Interface includes all the miscellaneous input/output interfaces: Codec IF, I^2S, Volume Control and S/PDIF In/Out interface. I^2S and S/PDIF IF will be accessed by Streaming Engine based on the fixed-rate interrupt (@48Khz).

FM801-AU Pin-Out

100 pin QFP Pin Diagram



FM801-AU I/O Pins Descriptions

Pin #	Pin Name	I/O Type	Description
1	GP2_X	B	Game port 2 joystick X-axis
2	GP1_X	B	Game port 1 joystick X-axis
3	GP2_BUTA	I	Game port 2 button A
4	GP1_BUTA	I	Game port 1 button A
5	VCC		3.3V Power for Core
6	PCI_INTA	O	PCI interrupt A
7	PSERIRQ	O	Serial IRQ
8	GND		Ground
9	PCI_RST	I	PCI system reset
10	PCI_CLK	I	PCI clock
11	PCI_GNT	I	PCI bus grant
12	GND		Ground
13	PCI_REQ	O	PCI bus request
14	PPME	O	PCI power management event
15	PAD[31]	B	PCI address/data
16	PAD[30]	B	PCI address/data
17	PAD[29]	B	PCI address/data
18	PAD[28]	B	PCI address/data
19	PAD[27]	B	PCI address/data
20	PAD[26]	B	PCI address/data
21	VCC		3.3V Power for PCI
22	PAD[25]	B	PCI address/data
23	GND		Ground for PCI
24	PAD[24]	B	PCI address/data
25	PCBE[3]	B	PCI command/byte enable
26	PIDSEL	I	PCI ID select
27	PAD[23]	B	PCI address/data
28	PAD[22]	B	PCI address/data
29	PAD[21]	B	PCI address/data
30	PAD[20]	B	PCI address/data
31	VCC		3.3V Power for PCI
32	PAD[19]	B	PCI address/data
33	GND		Ground for PCI
34	PAD[18]	B	PCI address/data
35	PAD[17]	B	PCI address/data
36	PAD[16]	B	PCI address/data
37	PCBE[2]	B	PCI command/byte enable

Pin #	Pin Name	I/O Type	Description
38	NC		No Connect
39	PFRAME	B	PCI frame
40	PIRDY	B	PCI initiator ready
41	PTRDY	B	PCI target ready
42	VCC		3.3V Power for PCI
43	PDEVSEL	B	PCI device select
44	PSTOP	B	PCI stop
45	PPERR	B	PCI parity error
46	PP_REQ	O	PC/PCI request
47	PPAR	B	PCI parity
48	PCBE[1]	B	PCI command/byte enable
49	PAD[15]	B	PCI address/data
50	VCC		3.3V Power for core
51	PAD[14]	B	PCI address/data
52	GND		Ground
53	GND		Ground
54	PAD[13]	B	PCI address/data
55	PAD[12]	B	PCI address/data
56	PAD[11]	B	PCI address/data
57	PAD[10]	B	PCI address/data
58	PAD[9]	B	PCI address/data
59	VCC		3.3V Power for PCI
60	PAD[8]	B	PCI address/data
61	PCBE[0]	B	PCI command/byte enable
62	GND		Ground
63	PAD[7]	B	PCI address/data
64	NC		No connect
65	PAD[6]	B	PCI address/data
66	PAD[5]	B	PCI address/data
67	PAD[4]	B	PCI address/data
68	PAD[3]	B	PCI address/data
69	PAD[2]	B	PCI address/data
70	VCC		3.3V Power for I/O
71	PAD[1]	B	PCI address/data
72	PAD[0]	B	PCI address/data
73	PCLKRUN/EE_CS/ EE_SCL	B	Clk Run/EEPROM chip select
74	PP_GNT	I	PC/PCI grant
75	SPDIFO/GPIO0	O	S/PDIF output
76	GND		Ground

Pin #	Pin Name	I/O Type	Description
77	XTAL_I	I	Main clock crystal in
78	XTAL_O	O	Main clock crystal out
79	I2LRCK/SPDIFI	I	I2s L/R clock
80	I2BCLK	I	I2s bit clock
81	I2SD	I	I2s serial data
82	VOL_UP/GPIO1/EE_CK	B	Volume up/EEPROM clock
83	VOL_DN/GPIO2/EE_DI/ EE_SDA	B	Volume down/EEPROM data in
84	MUTE/GPIO3/EE_DO	B	Volume mute/EEPROM data out
85	AC97_RST	O	CODEC reset
86	AC97_FS/EE_SEL	B	CODEC frame sync/EEPROM select
87	AC97_SDI	I	CODEC data in
88	NC		No connect
89	AC97_SCLK	I	CODEC clock
90	AC97_SDO/EE_EN	O	CODEC data out/EEPROM enable (tie HIGH for disable the EEPROM, tie LOW for enable the EEPROM)
91	AC97_CLK	O	CODEC main clock
92	AC97_SDI2	I	Data in from 2nd CODEC
93	MIDI_RXD	I	MIDI receiving data
94	GP1_BUTB	I	Game port 1 button B
95	GP2_BUTB	I	Game port 2 button B
96	GP1_Y	B	Game port 1 joystick Y-axis
97	GND		Ground
98	GP2_Y	B	Game port 2 joystick Y-axis
99	VCC		3.3V Power for I/O
100	MIDI_TXD	O	MIDI transmitting data

Pins Description in Detail:

I/O Type -- **B**-Bidirectional, **I**-Input, **O**-Output

PCI Interface

Name	Pin #	I/O	Description
PAD[31:0]	15:20 22, 24 27:30, 32 34:36,49 51, 54:58 60, 63 65:69 71:72	B	PCI address/data
PCBE[3:0]	25,37, 48,61	B	Multiplexed command/byte enable. These pins are inputs during slave operation and outputs during bus mastering operation.
PCI_CLK	10	I	PCI Bus clock. This clock times all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.
PCI_REQ	13	I	Bus master agent send out signal request access to bus
PCI_GNT	11	I	Bus master grant, active low. The system arbiter drives this pin to indicate to the device that access to the PCI bus has been granted.
PCI_INT	6	O	PCI interrupt A
PCI_RST	9	I	Reset
PCLKRUN/ EE_CS/ EE_SCL	73	B	PCI Clock Run/EPROM(93c57) chip select/EPROM (24c00) serial clock. The external EEPROM will load 6-words of data into Subsystem Vendor ID, Subsystem ID (func0), Subsystem ID (func1), Vendor ID, Device ID (func0), Device ID (func1) in this order.
PDEVSEL	43	B	Device Select, active low. The PCI bus target device drives this pin to indicate that it has decoded the address of the current transaction as its own chip select range.
PFRAME	39	B	Cycle frame, active low. The current PCI bus master drives this pin to indicate the beginning and duration of a transaction.
PIDSEL	26	I	ID select, active-high. This pin is used as a chip select during PCI configuration read and write cycles.
PIRDY	40	B	Initiator ready, active low. The current PCI bus master drives this pin to indicate that as the initiator it is ready to transmit or receive.
PPAR	47	B	Parity active high. This pin indicates even parity across{31:0} and PCBE{3:0} for both address and data phases. The signal is delay one PCI clock from either

			the address or data phase for which parity is generated.
PPERR	45	B	PCI Parity error check
PPME	14	O	Power management enable interrupt output to wake up the system.
PP_REQ	46	O	PC/PCI request
PSERIRQ	7	O	Serial IRQ
PSTOP	44	B	Stop transaction, active low. The current PCI bus target drives this pin active to indicate a request to the master to stop the current transaction.
PTRDY	41	B	Target ready, active low. The current PCI bus master drives this pin to indicate that as the target ready to transmit or receive.

AC97 Interface

Pin Name	Pin #	I/O	Description
AC97_RST	85	O	CODEC reset
AC97_FS	86	O	CODEC frame sync
AC97_SDI	87	I	CODEC data in
AC97_SCLK	89	I	CODEC clock
AC97_SDO	90	O	CODEC data out
AC97_CLK	91	O	CODEC main clock
AC97_SDI2	92	I	Data in from 2nd CODEC

I2S and S/PDIF IF

Pin Name	Pin #	I/O	Description
I2BCLK	80	I	I2S Bit clock
I2SD	81	I	I2S serial data
I2LRCK /SPDIFI	79	I	I2S left/right clock /SPDIF Input
SPDIFO /GPIO0	75	B	S/PDIF Data / GPIO[0]

Peripheral Interface

Pin Name	Pin #	I/O	Description
GP_X [1,2]	1,2	B	Game Port Data
GP_BUTA [1,2]	4,3	I	Game Port Data
GP_BUTB[1,2]	94,95	I	Dual Purpose pin, data input pin
GP_Y[1,2]	96,98	B	Game Port Data
MIDI_RXD	93	I	Receive Data
MIDI_TXD	100	O	Transmitting Data

Miscellaneous IO Pins

Pin Name	Pin #	I/O	Description
VOL_UP/GPIO1	82	I/B	VOL_UP is a volume increase input.
VOL_DN/ GPIO2/ EE_DI	83	I/B	VOL_DN is a volume decrease input. /GPIO(2)/EPROM(93c57) data in, or EPROM (24c00) data in and out.
MUTE/ GPIO3/ EE_DO	84	I/B	Volume mute/ GPIO(3)/EPROM(93c57) data out.
XTAL_I	77	I	Main clock crystal in
XTAL_O	78	O	Main clock crystal out
PSERIRQ	74	B	Special Protocol able to interface interrupts together in a single pin

Power and Ground

Pin Name	Pin #	I/O	Description
NC	38,64, 88		
VCC	5,21,31, 42,50,59, 70,99	Pwr	+3.3V power pins
GND	8,12,23,33,52, 53,62, 76,97	Pwr	Ground

Strap Selection Option

Pin Name	Pin #	I/O	Description
EE-EN	90	Low/High	0=E2PROM on board, 1=No E2PROM.
EE_SEL	86	Low/High	0=93c57, 1=24c00/24c01

FM801-AU PCI Configuration Registers

This section describes the summary and detailed description of *FM801-AU* Configuration registers. *FM801-AU* is a PCI multi-functions device (2 functions), Audio device(Function-0) and Game port device(Function-1). Therefore, there are 2 devices' configuration space defined in *FM801-AU*.

FM801-AU PCI Audio Device Configuration Registers Summary Table

Table PCI Audio Device (Function-0) Configuration Register Summary

Host Config Address	Host R/W	Power-on Value	Description
0x00~01	R	0x1319	Vendor ID (shadow of 0x98~99)
0x02~03	R	0x0801	Device ID (shadow of 0x9A~9B)
0x04~05	R/W	0x0000	PCI Command Register
0x06~07	R/W	0x0290	PCI Status Register
0x08	R	0xB2	Revision ID Register
0x09~0B	R	0x040100	Class Code (multimedia audio device)
0x0D	R/W	0x00	Latency Timer
0x0E	R	0x80	Header Type
0x10~13	R/W	0x00000001	I/O Base Register (offset=0x00~0x7F)
0x2C~2D	R	0x1319	Subsystem Vendor ID (shadow of 0x9C~9D)
0x2E~2F	R	0x1319	Subsystem ID (shadow of 0x9E~9F)
0x34	R	0xDC	Capabilities Pointer
0x3C	R/W	0x00	Interrupt Line Register
0x3D	R	0x01	Interrupt Pin Register (INTA#)
0x3E	R	0x04	Min Grant PCI Burst period
0x3F	R	0x28	Max Latency PCI grant period
0x40~41	R/W	0x907F	Legacy Audio Control
0x98~99	R/W	0x1319	Vendor ID Writeable
0x9A~9B	R/W	0x0801	Device ID Writeable
0x9C~9D	R/W	0x1319	Subsystem Vendor ID Writeable
0x9E~9F	R/W	0x1319	Subsystem ID Writeable
0xDC	R	0x01	Capability ID
0xDD	R	0x00	Next Item Pointer
0xDE~DF	R	0x0421	Power Management Capabilities
0xE0~E1	R/W	0x0000	Power Management Control/Status

FM801-AU PCI Audio Device Config. Registers Detailed Description

Vendor ID Register (R)

- Host Configuration Address: 0x00 – 0x01
- Power-on value: 0x1319
- Description: ForteMedia Vendor ID, can be programmed througth 0x98~99.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Device ID Register (R)

- Host Configuration Address: 0x02 – 0x03
- Power-on value: 0x0801
- Description: FM801-AU part number - 801, can be programmed througth 0x9A~9B.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

PCI Command Register (R/W)

- Host Configuration Address: 0x04 – 0x05
- Power-on value: 0x0000
- Description: Device capability on PCI operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						0	0	0	0	0	0	0	0	0	0

B0: Response to PCI I/O access - A value of 0 disables FM801-AU's response to I/O access. A value of 1 enables FM801-AU's response to I/O access.
B1: Response to PCI Memory access - A value of 0 disables FM801-AU's response to memory access. A value of 1 enables FM801-AU's response to memory access.
B2: Bus Master Capability - A value of 0 disables FM801-AU from generating PCI accesses. A value of 1 allows FM801-AU to behave as a bus master.
B3: Response to Special cycle - Zero always. Read only.
B4: Memory Write and Invalidate Command Generation - Zero always. Read only.
B5: VGA Palette Snoop - Zero always. Read only.
B6: PERR# Generation - If zero, FM801-AU ignore parity error it detects. If one FM801-AU will assert PERR# if parity error occurs.
B7: Address/Data stepping - Zero always. Read only.
B8: SERR# Generation - A value of 0 disables FM801-AU to generate SERR#. A value of 1 enables FM801-AU to generate SERR#.
B9: Fast Back-to-Back - Zero always. Read only.
B15~B10: Reserved.

PCI Status Register (R /W)

- Host Configuration Address: 0x06 – 0x07
- Power-on value: 0x0290
- Description: Status information for PCI bus related events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1				

B3~B0: Reserved
B4: PCI Power Management features appear in the standard configuration space header. Read Only.
B5: 66 MHz Capable- Zero always. Read only.
B6: UDF(User Definable Features) Support – Zero always
B7: Fast Back-to-Back - One always. Read only.
B8: PERR# active as Master - This bit is set when FM801-AU, as a master, asserts PERR# or detects the assertion of PERR# by other agent. This bit is cleared by writing an one to it.
B10~9: DEVSEL# Timing (Read only) -
0 0 = Fast
0 1 = Medium (Always)
1 0 = Slow
1 1 = reserved
B11: Signaled Target Abort - 0 = No, 1 = Yes. Write one to clear.
B12: Received Target Abort - 0 = No, 1 = Yes. Write one to clear.
B13: Received Master Abort - 0 = No, 1 = Yes. Write one to clear.
B14: Signaled System Error - 0 = No, 1 = Yes. Write one to clear.
B15: Detected Parity Error - 0 = No, 1 = Yes. Write one to clear.

Revision ID Register (R)

- Host Configuration Address: 0x08
- Power-on value: 0xB2
- Description: B2h for 4th revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	1	1	0	0	1	0

Programming Interface Register of Class Code (R)

- Host Configuration Address: 0x09
- Power-on value: 0x00
- Description: Specific register-level programming interface

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

Sub-class code Register of Class Code (R)

- Host Configuration Address: 0x0A
- Power-on value: 0x01(Func-0)
- Description: Sub-Class Code, Audio device

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	1

Base-class Code Register of Class Code (R)

- Host Configuration Address: 0x0B
- Power-on value: 0x04(Func-0)
- Description: Base Class Code, Multimedia device

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0								

Latency Timer Register (R/W)

- Host Configuration Address: 0x0D
- Power-on value: 0x00
- Description: Specifies the maximum number of PCI clocks that FM801-AU, as a bus master, will stay on the bus.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

Header Type Register (R)

- Host Configuration Address: 0x0E
- Power-on value: 0x80
- Description: Header type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	0	0	0	0	0	0

B7: Set to one to indicate multifunctional device.
B6~B0: Specify layout type of bytes 10h~3Fh; type “0” for bytes 10~3Fh, as defined in the PCI spec.

Base Address Register (R/W)

- Host Configuration Address: 0x10 – 0x13
- Power-on value: 0x00000001
- Description: Starting address of FM801-AU control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

B0: I/O Indicator - One always. Read only.
B1: reserved. Zero always. Read only.
B6~B2: Hardwired to zero. Read only.
B31~B7: Base Address - This address determines the starting address of 128 byte FM801-AU I/O registers mapped into PCI I/O space.

Subsystem Vendor ID (R)

- Host Configuration Address : 0x2C – 0x2D
- Power-on value : 0x1319
- Description : Subsystem Vendor ID. Can be written by external EPROM or programmed througth 0x9C~9D. This register is shared between 2 functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Subsystem ID (R)

- Host Configuration Address : 0x2E – 0x2F
- Power-on value : 0x1319
- Description : Subsystem ID. Can be written by external or programmed througth 0x9E~9F. This register is shared between 2 functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Capabilities Pointer (R)

- Host Configuration Address: 0x34
- Power-on value: 0xDC
- Description: This register is indicated where the PCI Power Management features appear in the standard configuration space header.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	1	0	1	1	1	0	0

Interrupt Line Register (R/W)

- Host Configuration Address: 0x3C
- Power-on value: 0x00
- Description: This register is used to communicate the interrupt line routing information.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	0

Interrupt Pin Register (R)

- Host Configuration Address: 0x3D
- Power-on value: 0x01(Func-0)
- Description: This register of Func-0 is hardwired to 0x01, which indicates that FM801-AU uses INTA# as interrupt pin.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1								

***** ***NOTE***: **Other registers not implemented will be read back as 00h**.

Min Grant Period for PCI burst (R)

- Host Configuration Address: 0x3E
- Power-on value: 0x04 (1 us)
- Description: This register is used to specify how long of a burst period the device needs(in ¼ microsecond unit). FM801-AU will use 1 us burst period.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	1	0	0

Max Latency for PCI Grant(R)

- Host Configuration Address: 0x3F
- Power-on value: 0x28 (10 us)
- Description: This register is used to specify how often the device needs(in ¼ microsecond unit) to gain access to the PCI bus. FM801-AU needs the PCI bus grant every 10 us.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0								

Legacy Audio Control Register (R/W)

- Host Configuration Address: 0x40 – 0x41
- Power-on value: 0x907F
- Description: This register provides control for independent enable/disable for each of the legacy audio subfunctions. This register can only be accessed through Func0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1

B0: Sound Blaster Enable. 1=Enable SB I/O positive decoding, 0=Disable.
B1: FM Synthesis Enable. 1=Enable FM Synthesis register positive decoding, 0=Disable.
B2: Game Port Enable. 1=Enable Game Port register positive decoding, 0=Disable.
B3: MPU-401 I/O Enable. 1=Enable MPU-401 register positive decoding, 0=Disable.
B4: MPU-401 IRQ Enable. 1=Enable IRQ specified in B13-B11, 0=Disable.
B5: I/O Address Alias Control. 1=10-bit address decoding, 0=16-bit address decoding.
B7~B6: SB DMA Channel Select. 00=DMA CH0, 01=DMA CH1, 10=Reserved, 11=DMA CH3.
B10~B8: SB IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.
B13~B11: MIDI I/O IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.
B14: Serial IRQ. 1=Serial IRQ enable, 0=Disbale.
B15: Global Legacy Audio Disable, supersede B4~B0. 1=Disable legacy audio, 0=Enable.

Vendor ID Writeable Register (R/W)

- Host Configuration Address: 0x98 – 0x99
- Power-on value: 0x1319
- Description: ForteMedia Vendor ID, the value of this register will also show in 0x00~01. This register shares with Func-1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Device ID Writeable Register (R/W)

- Host Configuration Address: 0x9A – 0x9B
- Power-on value: 0x0801
- Description: FM801-AU part number – 801. The value of this register will also show in 0x02~03.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Subsystem Vendor ID Writeable Register (R/W)

- Host Configuration Address : 0x9C – 0x9D
- Power-on value : 0x1319
- Description : Subsystem Vendor ID. The value of this register will also show in 0x2C~2D. This register shares with Func-1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Subsystem ID Writeable Register (R/W)

- Host Configuration Address : 0x9E – 0x9F
- Power-on value : 0x1319
- Description : Subsystem ID. The value of this register will also show in 0x2E~2F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Capabilities ID (R)

- Host Configuration Address: 0xDC
- Power-on value: 0x01
- Description: “01” indicates that the linked list item as being the PCI Power Management Registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	1

Next Item Pointer (R)

- Host Configuration Address: 0xDD
- Power-on value: 0x00
- Description: “00” indicates that there are no additional items in the Capabilities list.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

Power Management Capabilities (R)

- Host Configuration Address: 0xDE – 0xDF
- Power-on value: 0x0421(Func-0)
- Description: Describes information on the capabilities of the function related to power management.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1

B2~B0: Version number. PCI PM v1.0
B3: PME Clock. '0' indicates that no PCI clock is required to generated PME#.
B4: Reserved.
B5: Device Specific Initialization. '1' indicates that the function requires that a device specific initialization sequence following transition to the D0 uninitialized state.
B8~B6: Reserved.
B9(read only): D1 Support. 1=Yes, 0=No.
B10(read only): D2 Support. 1=Yes(Shutdown 24Mhz clock, I2S & AC97 DAC, ADC, Mixer), 0=No.
B15~B11: PME Support. For Func-0 device, power-on value is "00000", there's no PME support.

Power Management Control/Status (R/W)

- Host Configuration Address: 0xE0 – 0xE1
- Power-on value: 0x0000
- Description: This register is used to manage the PCI function's power management state as well as to enable/monitor power management events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0							0	0

B1~B0: Power state.
B7~B2: Reserved.
B8: PME Enable.
B12~B9: Data select. (Read only)
B14~B13: Data scale. (Read only)
B15: PME Status. Writing '1' to this bit will clear it and cause the function to stop asserting a PME. This bit defaults to '0' indicates the function does not support PME# generation from D3cold.

FM801-AU PCI GamePort Device Config. Registers Summary Table

Table PCI GamePort Device (Function-1) Configuration Register Summary

Host Config Address	Host R/W	Power-on Value	Description
0x00~01	R	0x1319	Vendor ID (shadow of 0x98~99)
0x02~03	R	0x0802	Device ID (shadow of 0x9A~9B)
0x04~05	R/W	0x0000	PCI Command Register
0x06~07	R/W	0x0290	PCI Status Register
0x08	R	0xB2	Revision ID Register
0x09~0B	R	0x098000	Class Code (Other input controller)
0x0D	R/W	0x00	Latency Timer
0x0E	R	0x80	Header Type
0x10~13	R/W	0x00000001	I/O Base Register (offset=0x00~0x0F)
0x2C~2D	R	0x1319	Subsystem Vendor ID (shadow of 0x9C~9D)
0x2E~2F	R	0x1319	Subsystem ID (shadow of 0x9E~9F)
0x34	R	0xDC	Capabilities Pointer
0x3C	R/W	0x00	Interrupt Line Register
0x3D	R	0x00	Interrupt Pin Register (INTB#)
0x3E	R	0x04	Min Grant PCI Burst period
0x3F	R	0x28	Max Latency PCI grant period
0x40~41	R	0x907F	Legacy Audio Control (only bit-2 is writeable)
0x98~99	R/W	0x1319	Vendor ID Writeable
0x9A~9B	R/W	0x0802	Device ID Writeable
0x9C~9D	R/W	0x1319	Subsystem Vendor ID Writeable
0x9E~9F	R/W	0x1319	Subsystem ID Writeable
0xDC	R	0x01	Capability ID
0xDD	R	0x00	Next Item Pointer
0xDE~DF	R	0x5221	Power Management Capabilities
0xE0~E1	R/W	0x0000	Power Management Control/Status

FM801-AU PCI GamePort Device Config. Registers Detailed Description

Vendor ID Register (R)

- Host Configuration Address: 0x00 – 0x01
- Power-on value: 0x1319
- Description: ForteMedia Vendor ID, can be programmed througth 0x98~99.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Device ID Register (R)

- Host Configuration Address: 0x02 – 0x03
- Power-on value: 0x0802
- Description: FM801-AU Gameport device ID – 802, can be programmed througth 0x9A~9B.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

PCI Command Register (R/W)

- Host Configuration Address: 0x04 – 0x05
- Power-on value: 0x0000
- Description: Device capability on PCI operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						0	0	0	0	0	0	0	0	0	0

B0: Response to PCI I/O access - A value of 0 disables FM801-AU's response to I/O access. A value of 1 enables FM801-AU's response to I/O access.
B1: Response to PCI Memory access - A value of 0 disables FM801-AU's response to memory access. A value of 1 enables FM801-AU's response to memory access.
B2: Bus Master Capability - A value of 0 disables FM801-AU from generating PCI accesses. A value of 1 allows FM801-AU to behave as a bus master.
B3: Response to Special cycle - Zero always. Read only.
B4: Memory Write and Invalidate Command Generation - Zero always. Read only.
B5: VGA Palette Snoop - Zero always. Read only.
B6: PERR# Generation - If zero, FM801-AU ignore parity error it detects. If one FM801-AU will assert PERR# if parity error occurs.
B7: Address/Data stepping - Zero always. Read only.
B8: SERR# Generation - A value of 0 disables FM801-AU to generate SERR#. A value of 1 enables FM801-AU to generate SERR#.
B9: Fast Back-to-Back - Zero always. Read only.
B15~B10: Reserved.

PCI Status Register (R /W)

- Host Configuration Address: 0x06 – 0x07
- Power-on value: 0x0290
- Description: Status information for PCI bus related events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1				

B3~B0: Reserved
B4: PCI Power Management features appear in the standard configuration space header. Read Only.
B5: 66 MHz Capable- Zero always. Read only.
B6: UDF(User Definable Features) Support – Zero always
B7: Fast Back-to-Back - One always. Read only.
B8: PERR# active as Master - This bit is set when FM801-AU, as a master, asserts PERR# or detects the assertion of PERR# by other agent. This bit is cleared by writing an one to it.
B10~9: DEVSEL# Timing (Read only) -
0 0 = Fast
0 1 = Medium (Always)
1 0 = Slow
1 1 = reserved
B11: Signaled Target Abort - 0 = No, 1 = Yes. Write one to clear.
B12: Received Target Abort - 0 = No, 1 = Yes. Write one to clear.
B13: Received Master Abort - 0 = No, 1 = Yes. Write one to clear.
B14: Signaled System Error - 0 = No, 1 = Yes. Write one to clear.
B15: Detected Parity Error - 0 = No, 1 = Yes. Write one to clear.

Revision ID Register (R)

- Host Configuration Address: 0x08
- Power-on value: 0xB2
- Description: B0h for 2nd revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	1	1	0	0	1	0

Programming Interface Register of Class Code (R)

- Host Configuration Address: 0x09
- Power-on value: 0x00
- Description: Specific register-level programming interface

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0								

Sub-class code Register of Class Code (R)

Host Configuration Address: 0x0A
Power-on value: 0x80(Func-1)
Description: Sub-Class Code, Other Input controller

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	1	0	0

Base-class Code Register of Class Code (R)

- Host Configuration Address: 0x0B
- Power-on value: 0x09(Func-1)
- Description: Base Class Code, Input device

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1								

Latency Timer Register (R/W)

- Host Configuration Address: 0x0D
- Power-on value: 0x00
- Description: Specifies the maximum number of PCI clocks that FM801-AU, as a bus master, will stay on the bus.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

Header Type Register (R)

- Host Configuration Address: 0x0E
- Power-on value: 0x80
- Description: Header type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	0	0	0	0	0	0	0

B7: Set to one to indicate multifunctional device.
B6~B0: Specify layout type of bytes 10h~3Fh; type “0” for bytes 10~3Fh, as defined in the PCI spec.

Base Address Register (R/W)

- Host Configuration Address: 0x10 – 0x13
- Power-on value: 0x00000001
- Description: Starting address of FM801-AU control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

B0: I/O Indicator - One always. Read only.
B1: reserved. Zero always. Read only.
B3~B2: Hardwired to zero. Read only.
B31~B4: Base Address - This address determines the starting address of 16 byte FM801-AU I/O registers mapped into PCI I/O space for Gameport.

Subsystem Vendor ID (R)

- Host Configuration Address : 0x2C – 0x2D
- Power-on value : 0x1319
- Description : Subsystem Vendor ID. Can be written by external EPROM or programmed througth 0x9C~9D. This register is shared between 2 functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Subsystem ID (R)

- Host Configuration Address : 0x2E – 0x2F
- Power-on value : 0x1319
- Description : Subsystem Vendor ID. Can be written by external EPROM or programmed througth 0x9E~9F. This register is shared between 2 functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Capabilities Pointer (R)

- Host Configuration Address: 0x34
- Power-on value: 0xDC
- Description: This register is indicated where the PCI Power Management features appear in the standard configuration space header.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								1	1	0	1	1	1	0	0

Interrupt Line Register (R/W)

- Host Configuration Address: 0x3C
- Power-on value: 0x00
- Description: This register is used to communicate the interrupt line routing information.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	0

Interrupt Pin Register (R)

- Host Configuration Address: 0x3D
- Power-on value: 0x00(Func-1)
- Description: The register of Func-1 is hardwired to 0x00, which indicates that FM801-AU Func-1 does not use interrupt pin

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

Min Grant Period for PCI burst (R)

- Host Configuration Address: 0x3E
- Power-on value: 0x04 (1 us)
- Description: This register is used to specify how long of a burst period the device needs(in ¼ microsecond unit). FM801-AU will use 1 us burst period.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	1	0	0

Max Latency for PCI Grant(R)

- Host Configuration Address: 0x3F
- Power-on value: 0x28 (10 us)
- Description: This register is used to specify how often the device needs(in ¼ microsecond unit) to gain access to the PCI bus. FM801-AU needs the PCI bus grant every 10 us.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0								

Legacy Audio Control Register (R)

- Host Configuration Address: 0x40 – 0x41
- Power-on value: 0x907F
- Description: This register provides control for independent enable/disable for each of the legacy audio subfunctions. This register can only be accessed through Func0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1

B0: Sound Blaster Enable. 1=Enable SB I/O positive decoding, 0=Disable.
B1: FM Synthesis Enable. 1=Enable FM Synthesis register positive decoding, 0=Disable.
B2 (R/W): Game Port Enable. 1=Enable Game Port register positive decoding, 0=Disable.
B3: MPU-401 I/O Enable. 1=Enable MPU-401 register positive decoding, 0=Disable.
B4: MPU-401 IRQ Enable. 1=Enable IRQ specified in B13-B11, 0=Disable.
B5: I/O Address Alias Control. 1=10-bit address decoding, 0=16-bit address decoding.
B7~B6: SB DMA Channel Select. 00=DMA CH0, 01=DMA CH1, 10=Reserved, 11=DMA CH3.
B10~B8: SB IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.
B13~B11: MIDI I/O IRQ Select. 000=IRQ5, 001=IRQ7, 010=IRQ9, 011=IRQ10, 100=IRQ11, others=Reserved.
B14: Serial IRQ. 1=Serial IRQ enable, 0=Disbale.
B15: Global Legacy Audio Disable, supersede B4~B0. 1=Disable legacy audio, 0=Enable.

Vendor ID Writeable Register (R/W)

Host Configuration Address: 0x98 – 0x99
Power-on value: 0x1319
Description: ForteMedia Vendor ID, the value of this register will also show in 0x00~01. This register shares with Func-0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Device ID Writeable Register (R/W)

- Host Configuration Address: 0x9A – 0x9B
- Power-on value: 0x0801
- Description: FM801-AU part number – 801. The value of this register will also show in 0x02~03.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Subsystem Vendor ID Writeable Register (R/W)

Host Configuration Address : 0x9C – 0x9D
Power-on value : 0x1319
Description : Subsystem Vendor ID. The value of this register will also show in 0x2C~2D. This register shares with Func-0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Subsystem ID Writeable Register (R/W)

- Host Configuration Address : 0x9E – 0x9F
- Power-on value : 0x1319
- Description : Subsystem ID. The value of this register will also show in 0x2E~2F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1

Capabilities ID (R)

- Host Configuration Address: 0xDC
- Power-on value: 0x01
- Description: “01” indicates that the linked list item as being the PCI Power Management Registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	0	0	0	1

Next Item Pointer (R)

- Host Configuration Address: 0xDD
- Power-on value: 0x00
- Description: “00” indicates that there are no additional items in the Capabilities list.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

Power Management Capabilities (R)

- Host Configuration Address: 0xDE – 0xDF
- Power-on value: 0x5221(Func-1)
- Description: Describes information on the capabilities of the function related to power management.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0	0	0	1	0	0	0	0	1

B2~B0: Version number. PCI PM v1.0
B3: PME Clock. ‘0’ indicates that no PCI clock is required to generated PME#.
B4: Reserved.
B5: Device Specific Initialization. ‘1’ indicates that the function requires that a device specific initialization sequence following transition to the D0 uninitialized state.

B8~B6: Reserved.
B9(read only): D1 Support. 1=Yes(Gameport power saving mode), 0=No.
B10(read only): D2 Support. 1=Yes, 0=No.
B15~B11: PME Support. For Func-0 device, power-on value is “00000”, there’s no PME support. For Func-1, it’s “01010” which indicates that PME# can be asserted from D3hot or D0.

Power Management Control/Status (R/W)

- Host Configuration Address: 0xE0 – 0xE1
- Power-on value: 0x0000
- Description: This register is used to manage the PCI function’s power management state as well as to enable/monitor power management events.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0							0	0

B1~B0: Power state.
B7~B2: Reserved.
B8: PME Enable.
B12~B9: Data select. (Read only)
B14~B13: Data scale. (Read only)
B15: PME Status. Writing ‘1’ to this bit will clear it and cause the function to stop asserting a PME. This bit defaults to ‘0’ indicates the function does not support PME# generation from D3cold.

FM801-AU PCI Control Registers

This section describes the summary and detailed description of *FM801-AU* I/O Control registers.

FM801-AU Audio Device Control Registers Summary Table

This section describes the summary and details of FM801-AU Audio Device Control Registers.

Table FM801-AU Audio Device Control Registers Summary Table

Host Offset	Host R/W	Power-on Value	Description
0x00~01	R/W	0x8808	PCM Out Volume
0x02~03	R/W	0x8808	FM Out Volume
0x04~05	R/W	0x8808	I2S Volume
0x06	R/W	0x00	Digital Recording Source Select
0x08~09	R/W	0xCA00	Playback Channel Control
0x0A~0B	R/W	-	Playback Channel Data Length
0x0C~0F	R/W	-	Playback Channel Buffer I System Starting Address
0x10~13	R/W	-	Playback Channel Buffer II System Starting Address
0x14~15	R/W	0xCA00	Capture Channel Control
0x16~17	R/W	-	Capture Channel Data Length
0x18~1B	R/W	-	Capture Channel Buffer I System Starting Address
0x1C~1F	R/W	-	Capture Channel Buffer II System Starting Address
0x22~23	R/W	0x0020	Codec Control
0x24~25	R/W	0x0003	I^2S Mode/SPDIF Control
0x26	R	0xXX	Volume Up/Dn/Mute Status
0x28	R/W	0x00	SRC/Mixer Test Control/DFC Status
0x29	R/W	0x00	I2C Control
0x2A~2B	R/W	0x00	Codec Index Register Command Port
0x2C~2D	R/W	-	Codec Index Register Data Port
0x30	R/W	-	MPU401 Data port
0x31	R/W	0x80	MPU401 Command/Status port
0x52~53	R/W	0x0E00	General Purpose I/O Control
0x70~71	R/W	0x0000	FM801-AU Blocks Power down control

FM801-AU Audio Device Control Registers Detailed Description

PCM Out Volume

- Host Offset Address: 0x00 - 0x01
- Power-on value: 0x8808
- Description: PCM Out Volume

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1			0	1	0	0	0				0	1	0	0	0

B15: PCM Out Mute.
B14~B13: Reserved.
B12~B8: PCM Right Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)
B7~B5: Reserved.
B4~B0: PCM Left Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)
* B15, B12~B8, B4~B0: read/write by host.

FM Out Volume

- Host Offset Address: 0x02 - 0x03
- Power-on value: 0x8808
- Description: FM Out Volume

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1			0	1	0	0	0				0	1	0	0	0

B15: FM Out Mute.
B14~B13: Reserved.
B12~B8: FM Right Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)
B7~B5: Reserved.
B4~B0: FM Left Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)
* B15, B12~B8, B4~B0: read/write by host.

I2S Volume

- Host Offset Address: 0x04 - 0x05
- Power-on value: 0x8808
- Description: I2S Volume

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1			0	1	0	0	0				0	1	0	0	0

B15: I2S Out Mute.
B14~B13: Reserved.
B12~B8: I2S Right Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)
B7~B5: Reserved.
B4~B0: I2S Left Channel Gain. 00000=+12db gain, 01000=0db gain, 11111=-34.5db gain. (each step corresponds to approximately 1.5db)
* B15, B12~B8, B4~B0: read/write by host.

Digital Recording Source Select

- Host Offset Address: 0x06
- Power-on value: 0x00
- Description: Digital Recording Source Select.

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
													0	0	0

B2~B0: Digital Recording Source Select. 000=Recording Data from ADC of AC97 primary codec, 001=FM, 010=I2S, 011=PCM, 100=Recording Data from ADC of AC97 secondary codec.
B7~B3: Reserved.
* B2~B0: read/write by host.

Playback Channel Control

- Host Offset Address: 0x08 – 0x09
- Power-on value: 0xCA00
- Description: Direct Sound Playback Channel Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0

B0: DFC/PFIFO data empty. 1=Empty, 0=Not empty.
B1: Current buffer I transfer is the last transfer. 0=No, 1=Yes.
B2: Current buffer II transfer is the last transfer. 0=No, 1=Yes.
B4~B3: SRC Output sampling rate. 00=48KHz, 01=44.1KHz, 10=32KHz, 11=reserved.
B5: Channel Action. 0=Stop Transfer, 1=Start Transfer.[1]
B6: Channel Pause. 0=Normal, 1=Transfer Pause. (To pause, bit-5 has to remain '1')
B7: Channel Stop Point. 0=At the end of current buffer, 1=Immediately stop when receiving Stop command.
B11~B8: Sampling Rate. 0000=5.5Khz, 0001=8Khz, 0010=9.6Khz, 0011=11.025Khz, 0100=16Khz, 0101=19.2Khz, 0110=22.05Khz, 0111=32Khz, 1000=38.4Khz, 1001=44.1Khz, 1010=48Khz.
B13~B12: Channel Format[2]. 00=2 Ch, 01=4 Ch, 10=6 Ch, 11=MS 6-Ch.
B14: Data Format. 0=8-bit unsigned, 1=16-bit signed.
B15: Stereo/Mono. 0=Mono, 1=Stereo.
* B15~B5, B2~B1: read/write by host. B0:read only.

Playback Channel Data Length/Current Count

- Host Offset Address: 0x0A - 0x0B
- Power-on value: 0xXXXX
- Description: Direct Sound Playback Channel Data Length & Current Count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

[1] When 'stop transfer' command is received, current buffer transfer has to be finished before PCI actually stops sending any transfer request so that Sw driver can track where the current pointer is. When it overruns, the DFC has to overwrite the old data with the latest data.
[2] 4-channel format will be: L/R/LS/RS. 6-channel format will be: L/R/LS/RS/CT/LFE.

B15~B0(write): DS Channel Data Length for buffer I and II (Have to be the same size for both buffers). The actual transfer count will be this register value plus 1.
B15~B0(read): DS Channel Data Current Remaining Count.(not available until playback starts)
* B15~B0: read/write by host.

Playback Channel Buffer I System Starting Address

- Host Offset Address: 0x0C - 0x0F
- Power-on value: 0xXXXX
- Description: Direct Sound Playback Channel Buffer I System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): DS Playback Channel Buffer I System Starting Address.
B31~B0(read): DS Playback Channel Buffer I current address.
* B31~B0: read/write by host.

Playback Channel Buffer II System Starting Address

- Host Offset Address: 0x10 - 0x13
- Power-on value: 0xXXXX
- Description: Direct Sound Playback Channel Buffer II System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): DS Playback Channel Buffer II System Starting Address.
B31~B0(read): DS Playback Channel Buffer II current address.
* B31~B0: read/write by host.

Capture Channel Control

- Host Offset Address: 0x14 – 0x15
- Power-on value: 0xCA00
- Description: Direct Sound Capture Channel Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0		1	0	1	0	0	0	0	0	0	0	0	

B0: Reserved.
B1: Current buffer I transfer is the last transfer. 0=No, 1=Yes.
B2: Current buffer II transfer is the last transfer. 0=No, 1=Yes.
B4~B3: SRC Input Sampling Rate. 00=48KHz, 01=44.1KHz, 10=32KHz, 11=reserved.
B5: Channel Action. 0=Stop Transfer, 1=Start Transfer[3].
B6: Channel Pause. 0=Normal, 1=Transfer Pause. (To pause, bit-5 has to remain '1')

[3] When 'stop transfer' command is received, current buffer transfer has to be finished before PCI actually stops sending any transfer request so that Sw driver can track where the current pointer is. When it overruns, the DFC has to overwrite the old data with the latest data.

B7: Channel Stop Point. 0=At the end of current buffer, 1=Immediately stop when receiving Stop command.
B11~B8: Sampling Rate. 0000=5.5Khz, 0001=8Khz, 0010=9.6Khz, 0011=11.025Khz, 0100=16Khz, 0101=19.2Khz, 0110=22.05Khz, 0111=32Khz, 1000=38.4Khz, 1001=44.1Khz, 1010=48Khz.
B12: Reserved.
B13: Capture SRC bypass enable. 1=Bypass mode, 0=Normal.
B14: Data Format. 0=8-bit unsigned, 1=16-bit signed.
B15: Stereo/Mono. 0=Mono, 1=Stereo.
* B15~B14, B11~B5, B2~B0: read/write by host.

Capture Channel Data Length/Current Count

- Host Offset Address: 0x16 - 0x17
- Power-on value: 0xXXXX
- Description: Capture Channel Data Length & Current Count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B15~B0(write): Capture Channel Data Length for buffer I and II (Have to be the same size for both buffers). The actual transfer count will be this register value plus 1.
B15~B0(read): DS Channel Data Current Remaining Count.(not available until capture starts)
* B15~B0: read/write by host.

Capture Channel Buffer I System Starting Address

- Host Offset Address: 0x18 - 0x1B
- Power-on value: 0xXXXX
- Description: Capture Channel Buffer I System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): Capture Channel Buffer I System Starting Address.
B31~B0(read): Capture Channel Buffer I current address.
* B31~B0: read/write by host.

Capture Channel Buffer II System Starting Address

- Host Offset Address: 0x1C - 0x1F
- Power-on value: 0xXXXX
- Description: Direct Sound Playback Channel Buffer II System Starting Address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B31~B0(write): Capture Channel Buffer II System Starting Address.
B31~B0(read): Capture Channel Buffer II current address.
* B31~B0: read/write by host.

Codec Control

- Host Offset Address: 0x22 - 0x23
- Power-on value: 0x0000
- Description: Audio Codec Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0	0	0	0	0	0	1					

B4~B0: Reserved.
B5: Codec Cold Reset. 1=Cold Reset, 0=Normal.
B6: AC'97 Warm Reset. 1=Warm Reset, 0=Normal.
B7: 2-Ch to 4-Ch copy mode enable. 1=Enable, 0=Disable.
B8: AC'97 ATE Test Mode. 1=ATE Test Mode On, 0=Normal.
B9: AC'97 GPIO Mode is enable. 1=Enable, 0=Disable.
B10: AC97 16/18bit mode. 1=18-bit, 0=16-bit.
B11: AC97 Variable Sample Rate support. 1=Yes, 0=No.
B15~B12: Reserved.
*B11~B5: read/write by Host.

I2S Mode / SPDIF Control

- Host Offset Address: 0x24 – 0x25
- Power-on value: 0x0003
- Description: I^2S Serial Port Data Format Mode and SPDIF Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					0	0	0	0	0	0				1	1

B1~B0: I2S Format. 00, 01=DAC, Digital Format. 10=ADC, DSP Serial Port, 11=I2S Mode.
B4~B2: Reserved.
B5: I2S Sample Rate Source Select. 1=Sw Control, 0=Hw Logic Detect.
B7~B6: I2S Sampling Rate. 00=48Khz, 01=44.1Khz, 10=32Khz.
B8: I2S Mode/SPDIF Data In mode. I-SPDIF Data In Mode. 0=I2S Mode.
B9: SPDIF Data Out Pass Through. 1=AC-3 Raw Data Pass Through Mode. 0=Decoded Audio Data Mode.
B10: SPDIF Data In Pass Through. 1=AC-3 Raw Data Pass Through Mode. 0=Decoded Audio Data Mode.
B15~B11: Reserved.
*B10~B5, B1~B0: read/write by Host.

Volume Up/Dn/Mute Status & Volume Counter Enable

- Host Offset Address: 0x26
- Power-on value: 0xXX
- Description: Volume Up/Dn/Mute Status(Read) & Volume Counter Enable(Write).

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
													0	0	0

B0: Volume Up button is pushed. 1=Pushed, 0=No activity.
B1: Volume Down button is pushed. 1=Pushed, 0=No activity.
B2: Volume Mute button is pushed. 1=Pushed, 0=No activity.
B7~B3: Reserved.
* B2~B0: read only by host.

** When write to this register will enable the volume control counter to start counting.
** When both volume up and down are pushed at the same time, it will mute the volume.

I2C Control

- Host Offset Address : 0x29
- DSP I/O Address : N/A
- Power-on value : 0x00
- Description : I2C Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								

B8: I2C Clock output.
B9: I2C Data output.
B10: I2C Chip select. 1=Enable, 0=Disable.
B11: I2C Port Enable. 1=Enable, 0=Disable.
B12: I2C read. 1=Read from EPROM, 0=Disable.
B13: I2C read from beginning of EPROM.
B14: I2C 4 bytes data are ready. 1=Ready, 0=Not ready.
B15: I2C Data Input. 1=Enable, 0=Disable.
* B15~B14: read only by host. B11~B8: read/write by host.

Codec Index Register Command Port

- Host Offset Address: 0x2A – 0x2B
- Power-on value: 0x0000
- Description: Audio Codec Index Register Command Port.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				0	0	0	0	0	-	-	-	-	-	-	-

B6~B0: Codec Index Address.
B7: Read/Write Command. 0=Write, 1=Read.
B8: Data Port Valid Flag. 0=Invalid, 1=Valid.
B9: Command Port Status. 0=Ready, 1=Busy.
B11~B10: Codec ID been programmed.
* B9~B8: read only. B11~B10, B7~B0: read/write by host.

Codec Index Register Data Port

- Host Offset Address: 0x2C - 0x2D
- Power-on value: 0xXXXX
- Description: Audio Codec Index Register Data port

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B15~B0: Codec Register data port.
* B15~B0: read/write by host.

MPU401 Data Port

- Host Offset Address: 0x30
- Power-on value: N/A

- Description: MPU401 Data Port.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								-	-	-	-	-	-	-	-

B7~B0: MPU401 Data [7:0]
* B7~B0: read/write by Host.

MPU401 Command/Status Port

- Host Offset Address: 0x31
- Power-on value: 0x80
- Description: MPU401 Command/Status Port.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0								

B15~B8(Write): MPU401 Command [7:0]
* B15~B8: Write by Host.
B15(Read): MIDI Data Valid. 1=Not Valid, 0=Valid.
B14(Read): MIDI Cmd/Data Port Status. 1=Busy, 0=Not Busy.
B13~B10(Read): MIDI Valid Data Count.
B9~B8(Read): Reserved.
* B13~B10: read by Host.

General Purpose I/O Control

- Host Offset Address: 0x52 – 0x53
- Power-on value: 0x0E00
- Description: General Purpose I/O Pins Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0					0	0	0	0

B3~B0: General Purpose I/O [3:0] (Go through FM801-AU)
B7~B4: Reserved.
B11~B8: General Purpose I/O [3:0] Configuration. 1=Input, 0=Output.
B15~B12: General Purpose Output Pins Select [3:0]. 1=GPIO select, 0=Other functions.
* B15~B0: read/write by Host.

FM801-AU Blocks Power Down Control

- Host Offset Address: 0x70 - 0x71
- Power-on value: 0x0000
- Description: This register will power down the Hw blocks in FM801-AU.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							0								

B15: Shutdown 24.576Mhz to Audio block. 1=Shutdown, 0=Normal.
B14~B9: Reserved.
B8: PCI Clock can be turn off. 1=Ready, 0=Not ready to power down.
* B15, B8: read/write by host

FM801-AU GamePort Device Control Registers Summary Table

This section describes the summary and details of FM801-AU GamePort Control Registers.

Table FM801-AU GamePort Device Control Registers Summary Table

Host Offset	Host R/W	Power-on Value	Description
0x00~01	R/W	-	Conventional Game Port
0x02~03	R	-	Game Port J1-X Counter
0x04~05	R	-	Game Port J1-Y Counter
0x06~07	R	-	Game Port J2-X Counter
0x08~09	R	-	Game Port J2-Y Counter
0x0D	R/W	0x6000	Game Port Control

FM801-AU GamePort Device Control Registers Detailed Description

Conventional Game Port

- GamePort Host Offset Address: 0x00 – 0x01
- Power-on value: N/A
- Description: Game Port. Write any value to this port will reset the register value. This register is an alias of the legacy gameport register at 0x200~0x201.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

B8, B0: Joystick 1P X-axis.
B9, B1: Joystick 1P Y-axis.
B10, B2: Joystick 2P X-axis.
B11, B3: Joystick 2P Y-axis.
B12, B4: Joystick 1P Button A.
B13, B5: Joystick 1P Button B.
B14, B6: Joystick 2P Button A.
B15, B7: Joystick 2P Button B.
* B15~B8, B7~B0: read/write by Host

Game Port J1-X Counter

- GamePort Host Offset Address: 0x02 - 0x03
- Power-on value: N/A
- Description: Game Port Joystick 1P X-counter. Write any value to “Conventional game port”(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-		-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 1P X-axis counter value.
B13: Reserved.
B14: Joystick 1P Button A.
B15: Joystick 1P Button B.
* B15~B14, B12~B0: read only by Host.

Game Port J1-Y Counter

- GamePort Host Offset Address: 0x04 - 0x05
- Power-on value: N/A
- Description: Game Port Joystick 1P Y-counter. Write any value to "Conventional game port"(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 1P Y-axis counter value.
B15~B13: Reserved.
* B12~B0: read only by Host.

Game Port J2-X Counter

- GamePort Host Offset Address: 0x06 - 0x07
- Power-on value: N/A
- Description: Game Port Joystick 2P X-counter. Write any value to "Conventional game port"(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-		-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 2P X-axis counter value.
B13: Reserved.
B14: Joystick 1P Button A.
B15: Joystick 1P Button B.
* B15~B14, B12~B0: read only by Host.

Game Port J2-Y Counter

- GamePort Host Offset Address: 0x08 - 0x09
- Power-on value: N/A
- Description: Game Port Joystick 2P Y-counter. Write any value to "Conventional game port"(0x00) will reset the register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			-	-	-	-	-	-	-	-	-	-	-	-	-

B12~B0: Game Port Joystick 2P Y-axis counter value.
B15~B13: Reserved.
* B12~B0: read only by Host.

Game Port Control

- GamePort Host Offset Address: 0x0D
- Power-on value: 0x6000
- Description: Game Port Control.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	0	0	0	0			

B2~B0: Reserved.
B3: Game Port trigger PME Enable. 1=Enable, 0=Disable.

B4: Shutdown 24.576MHz to GamePort. 1=Shutdown. 0=Normal.
B5: GamePort INT Status/Clear. (Read) 1=GamePort is triggered. 0=Not triggered. Write "1" to this bit will clear the status, write "0" to this bit will have no effect.
B7~B6: GamePort Discharge Time. 00=1us. 01=2us. 10=4us. 11=8us.
B9~B8: Game Port Movement Resolution. 00=9-bit, 01=8-bit, 10=7-bit, 11=6-bit.
B10: Intelligent Game Port Mode Enable. 1=On(Motion/push button auto detect), 0=Off.
B11: Func1 PCI clock can be turned off. 1=Ready. 0=Not ready to power down.
B12: Game Port Power Saving Mode. 1=On(No discharge after charging to 1), 0=Off.
B13: Game port Joystick 1 enable/disable. 1=Enable, 0=Disable.
B14: Game port Joystick 2 enable/disable. 1=Enable, 0=Disable.
B15: Game Port Sw reset. 1=Reset, 0=Normal.
*B15~B3: read/write by host.

TIMING REQUIREMENT

PCI Timing Requirement

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{PCKP}	PCI Bus Clock Period	30			ns	
t_{PCKL}	PCI Bus Clock Low Time	12			ns	
t_{PCKH}	PCI Bus Clock High Time	12			ns	
t_{SPCI}	Input Setup Time to PCI_CLK				ns	
t_{HPCI}	Input Hold Time to PCI_CLK		20		ns	
t_{PPCI}	Output propagation delay from PCI_CLK				ns	0 pf load 50 pf load
T_val	PCI clock to bus valid delay	7		17	ns	
T_su	Input set up time to clock	2			ns	
T_hold	Input hold time from clock	0			ns	

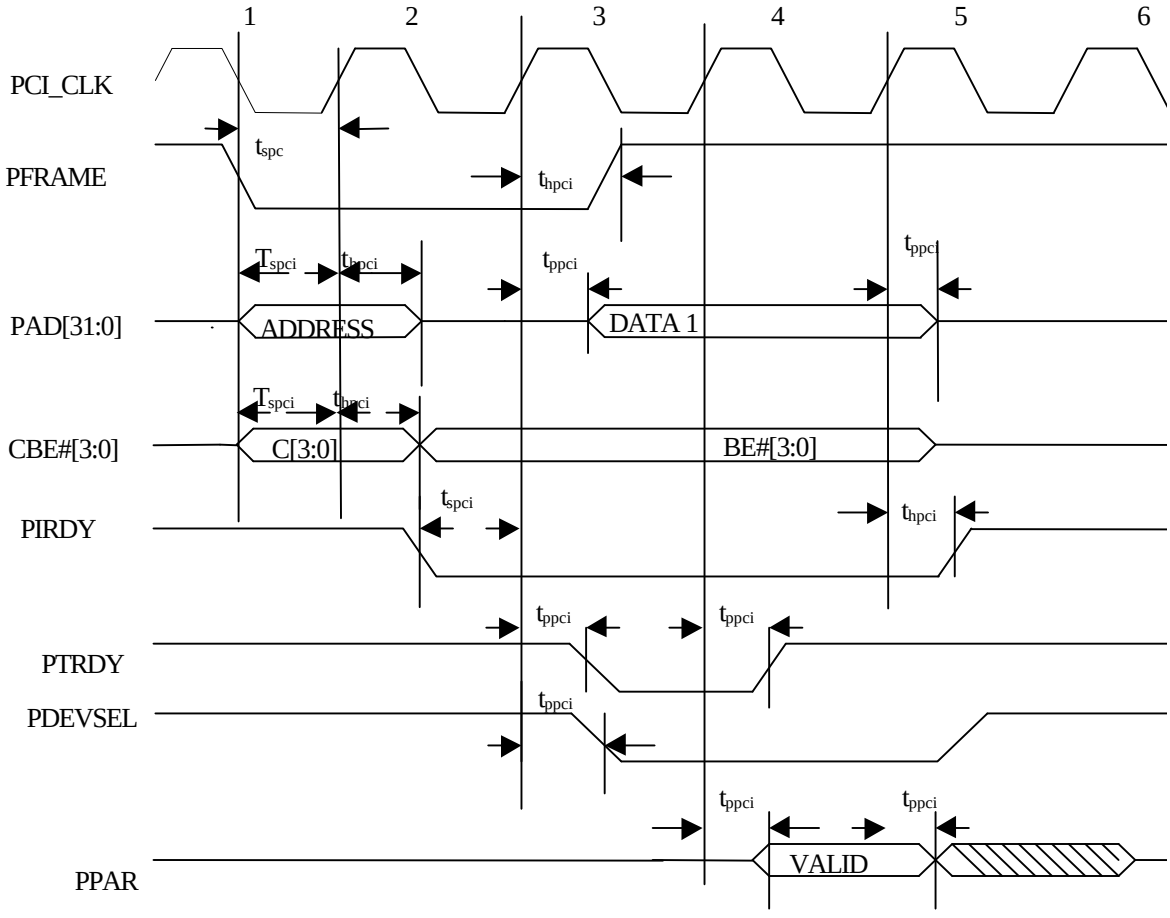


Figure: PCI Bus Timing (I/O Read Operation)

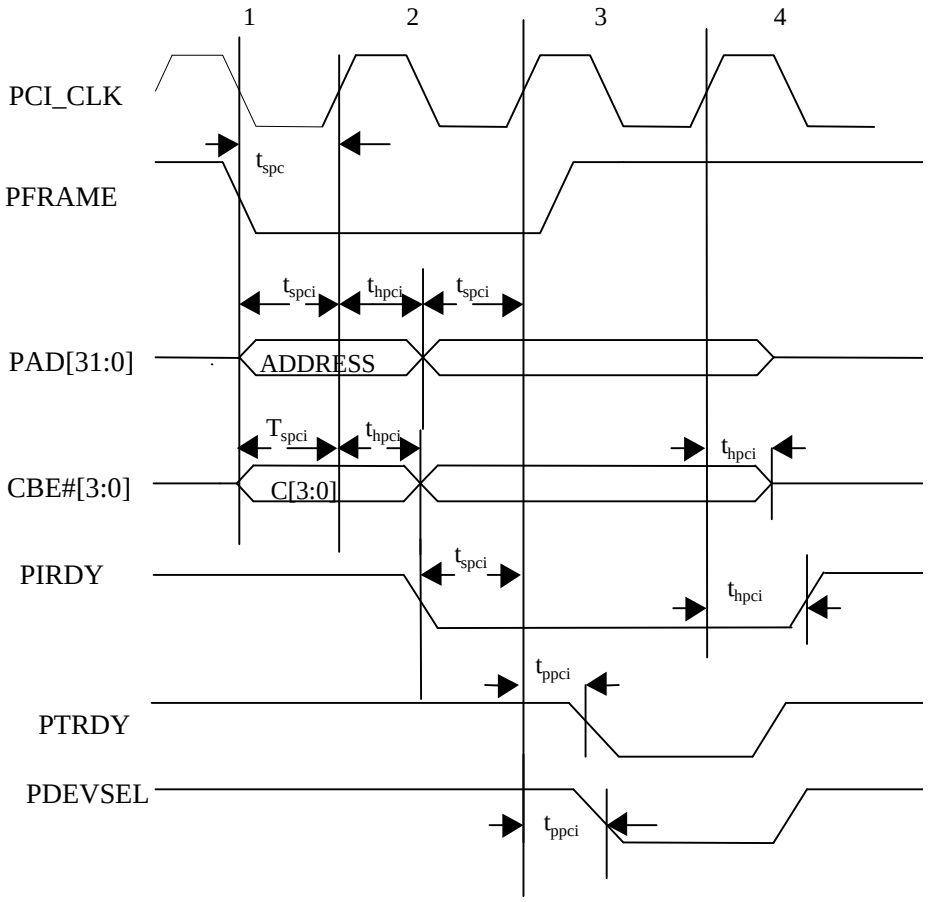
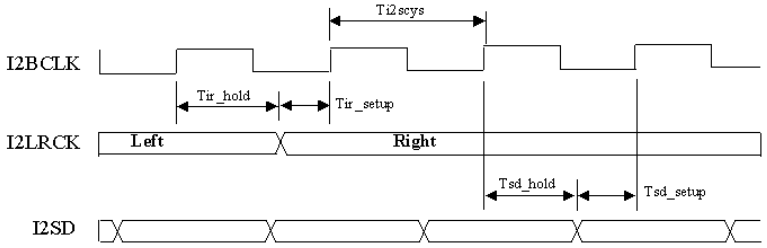


Figure: PCI Bus Timing (I/O Write Operation)

I2S TIMING (I/O OPERATION)

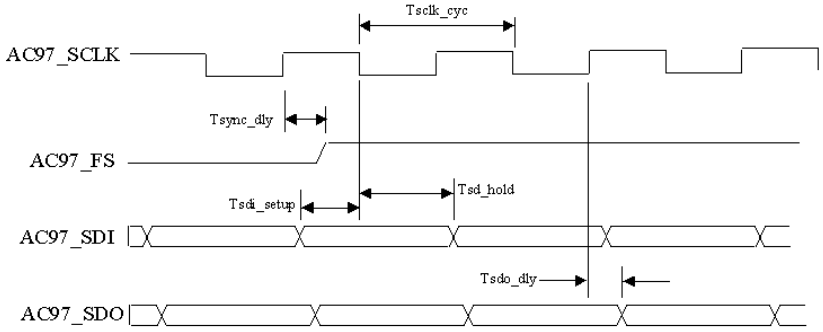
Symbol	Parameter	Min.	Typ	Max.	Units	Notes
Ti2scyc	I2S clock cycle time	54				
Tir_setup	LRCK setup	10				
Tir_hold	LRCK hold time	2				
Tsd_setup	I2S Data setup time	10				
Tsd_hold	I2S Data hold time	2				



I2S Data Port Timing

AC-Link TIMING

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
Tsdi_setup	AC97 SDI setup time	15				
Tsdi_hold	AC97 SDI hold time	5				
Tsdo_dly	SCLK positive-dege to SDO ready	6		15		
Tsync_dly	SCLK positive-edge to SYNC ready	6		15		
Tsclk_cyc	SCLK cycle time		81.38			



AC-Link Timing

ABSOLUTE MAXIMUM RATINGS

The values listed below are stress ratings only. Functional operation at the maximum ratings is not recommended or guaranteed. The device's reliability is affected if the operated for extended periods a maximum ratings. Electrostatic discharge damage may result from high static voltages or electric fields.

Symbol	Parameter	Min	Max	Units
DV_{DD}	Digital Power Supply	-0.3	5.5	V
V_{ID}	Digital Input Voltage	-0.3	5.5	V
V_{ESD}	ESD Tolerance	2000		V
T_{OPER}	Operating Temperature	0	+70	^oC
T_{STG}	Storage Temperature	-65	+150	^oC
P_{DMAX}	Maximum Power Dissipation at T_j=125^oC		1000	mW

DIGITAL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	units
l_{il}	Low level Input Current	$V_{in}=V_{ss}$	-10		10	uA
l_{ih}	High level Input Current	$V_{in}=V_{dd}$	-10		10	uA
l_{oz}	Tristate Output Leakage Current	$V_{out}=V_{dd}/V_{ss}$	-10		10	uA
V_{il}	Low level Input Voltage	TTL-static			0.8	V
V_{ih}	High level Input Voltage	TTL-static	2.0			V
V_{ol}	Low level Output Voltage	TTL-static			0.4	V
V_{oh}	High level Output Voltage	TTL-static	2.4			V
C_{in}	Input Capacitance	1Mhz @ 0V			10	pF
C_{out}	Output Capacitance	1Mhz @ 0V			10	pF

ELECTRICAL CHARACTERISTICS

AC-Link Signals DC Characteristic

Symbol	Parameter	Min.	Max.	Units
V_{in}	Input Voltage Range	Vss	5.5	V
V_{il}	Low level input Voltage	-	0.8	V
V_{ih}	High level input Voltage	2.0	-	V
V_{oh}	High level output Voltage	2.4	-	V
V_{ol}	Low level output Voltage	-	0.4	V
-	Input leakage Current	-1	1	uA
-	Output leakage Current	-1	1	uA

Note: T_A=^{o}C to 70^{o}C; V_{DD}= 3.3V+-10%; V_{SS}=0V

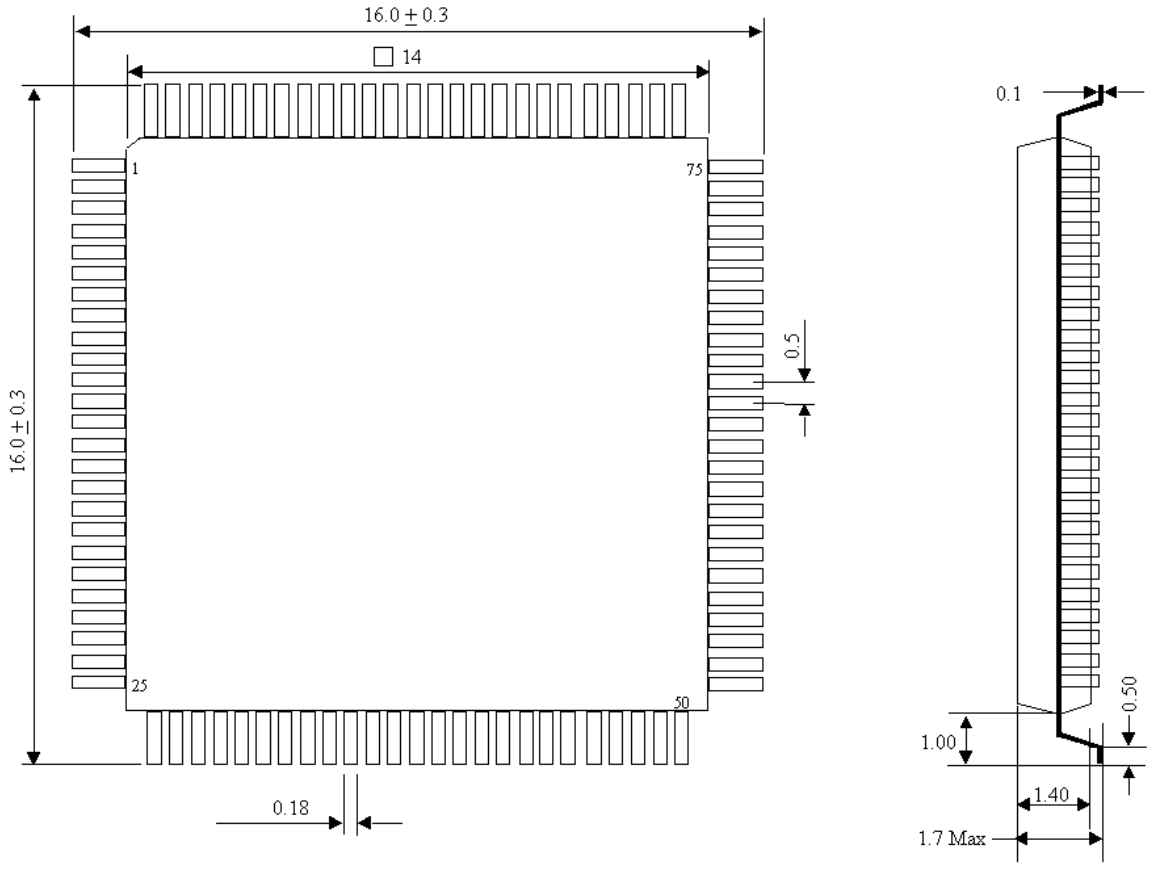
ELECTRICAL CHARACTERISTICS FOR 3V POWER SUPPLY

The FM801-AU device operates properly when the case Temperature (Tc) is within the specified temperature range of 0oC to 70oC

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Voltage (LV-TTL level)	V_{LHT} V_{LLT}	- -	2.0 Vss	- -	5.5 0.8	V V
Schmidt Trigger Voltage	Vtt+ Vtt- Delta Vtt	Vdd=Max Vdd=Min Vdd=Min	-1.1 0.6 0.1	- - -	2.4 1.8 -	V V V
Output Voltage	V_{OHT}	Ioh=-2/6/12mA	Vdd-0.4	-	-	V
Output Voltage	V_{ohc}	Ioh=-200uA	Vcc-0.1	-	-	V
PCI (Vcc=3.3V+/-0.3v)	V_{ih} V_{il}	Vdd=Max Vdd=Min	1.71	- -	- 0.98	V V
Input Leakage(I) Output Leakage(I)	I_{li} I_{lo}	- At High Impedance	- -	- -	1 1	uA uA
Pull_Down Resistance	R	Vin=Vdd	40	100	240	K-ohm
Supply Current	I_{dd}	At operating State	-	25	40	ma

PACKAGING DIMENSIONS

100 pin QFP – Plastic Low Profile Quad Flat Pack,
14 mm x 14 mm x 1.4 mm Body.
Units: mm



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