# PMAG-BA TURBOchannel Color Frame Buffer Functional Specification

**Revision 1.2**

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## Revision History

| Date | Version | Content/Changes |
|---|---|---|
| 29 Aug 89 | 1.0 | Release copy |
| 06 Nov 89 | 1.1 | Added Interrupt Ena Description |
| | | Added cursor coordinate data |
| 24 Aug 90 | 1.1 | Cleaned up for external release |

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## 1. PMAG-BA TURBOchannel Color Frame Buffer Module

This is the functional specification for the PMAG-BA Module. The PMAG-BA Module contains the following subsystems:

- 1024 KBytes of VRAM Color Frame Buffer and associated I/O Control Logic
- Bt459 Cursor/RAMDAC chip
- 64 KByte ROM
- Video Control Logic (timing and refresh)

The PMAG-BA Module acts as a slave only device on the TURBOchannel and may reside in any one (or more) of the three DS5000/200 option slots.

The I/O Control Logic manages access to the VRAM CFB, ROM, IReq Control Address, and Bt459. The I/O Control Logic supports Page-Mode reads and writes to the VRAM.

The Bt459 monolithic Cursor/RAMDAC chip provides all the necessary functionality to interface the CFB to the video monitor.

An onboard ROM is provided for diagnostic code and fonts storage.

The Video Control Logic manages VRAM refresh, generates video interrupts, SYNC and BLANK monitor timing, and controls data transfers between the CFB and the Bt459.

## 2. Address Map

The DECstation 5000/200 allocates the top 32 MBytes of physical address space to the I/O subsystems. The 32 MByte I/O region is further divided into 8 regions of 4 MBytes each, for each one of the eight subsystems that may exist on the TURBOchannel. Refer to the *TURBOchannel Hardware Specification* for further details on the bus (order number EK-369AA-OD-005). Table 2-1 lists these regions.

**Table 2-1: DECstation 5000/200 I/O Address Space**

| Address Range | Size (MBytes) | Sub-Systems |
|---|---|---|
| 0x1FC00000..0x1FFFFFFF | 4.0 | System support |
| 0x1F800000..0x1FBFFFFF | 4.0 | System module embedded I/O slot 6 |
| 0x1F400000..0x1F7FFFFF | 4.0 | System module embedded I/O slot 5 |
| 0x1F000000..0x1F3FFFFF | 4.0 | Reserved |
| 0x1EC00000..0x1EFFFFFF | 4.0 | Reserved |
| 0x1E800000..0x1EBFFFFF | 4.0 | Option Connector 2 (on P/S side) |
| 0x1E400000..0x1E7FFFFF | 4.0 | Option Connector 1 |
| 0x1E000000..0x1E3FFFFF | 4.0 | Option Connector 0 |

The PMAG-BA Module may reside in any of the three option connector slots. The 4 MByte address space on the PMAG-BA Module is further divided as shown in Table 2-2

**Table 2-2: PMAG-BA Module Address Map**

| Address Range | Subsystem |
|---|---|
| 0xbb+000000..0xbb+0FFFFF | VRAM Frame Buffer |
| 0xbb+100000..0xbb+1FFFFF | VRAM Frame Buffer |
| 0xbb+200000..0xbb+2FFFFF | Bt459 |
| 0xbb+300000..0xbb+37FFFF | IReq Control Address |
| 0xbb+380000..0xbb+3BFFFF | PMAG-BA Diagnostic ROM |
| 0xbb+3C0000..0xbb+3FFFFF | PMAG-BA Diagnostic ROM(*) |

(*) Writes to the rom address range cause reset to be asserted to the video clock chip.

The PMAG-BA subsystem occupies the entire 4 MByte region. References to any address within this region will always be acknowledged. "bb" is the base address of the I/O slot in which the PMAG-BA Module resides.

The R3000 CPU is configured for little-endian byte order. All address space descriptions in this document are correspondingly little-endian.

## 3. Functional Description

### 3.1. Color Frame Buffer

The PMAG-BA Module contains a 1024-by-864 pixel, 8-plane Color Frame Buffer (CFB). The CFB appears as a 256-K-by-32-bit region of memory in the PMAG-BA Module's address space. The CFB is organized as 1024-by-1024 pixels, of which the upper 1024-by-864 pixels are displayed. Each word of the CFB contains 4 consecutive pixels of a scan line. Each scan line of the display corresponds to 256 words. The stride between displayed columns is 1024 pixels (1024 bytes). In a given word, pixels are displayed from byte 0 through byte 3 (word 0xbb+000000 or 0xbb+100000, byte 0 is the upper-left-hand pixel on the display). The unused portions of the CFB may be used as a general purpose storage area. Unlike memory, however, the CFB is not ECC or parity protected.

The CFB supports byte, half-word, tri-byte, and word writes. Masked reads are treated as full word reads, with the R3000 performing the appropriate byte masking and alignment. In addition the CFB is operated in Page Mode as long as addresses generated by the host are within the same page (a page is defined as 2048 bytes). Page Mode writes to the CFB complete at a rate of 4 IO-Bus cycles per word (peak write BW of 25 MBytes/second at a nominal 40 Nanoseconds per IO-Bus cycle). Non Page Mode writes to the CFB complete at a rate of 8 cycles per word (peak write BW of 12.5 MBytes/second). Page Mode reads to the CFB complete at a rate of 6 cycles per word (peak read BW of 16.67 MBytes/second). Non Page Mode reads to the CFB complete at a rate of 10 cycles per word (peak read BW of 10 MBytes/second). CFB access during Refresh activity will increase access latency by 20 additional cycles.

### 3.2. Bt459 RAMDAC

The Bt459 RAMDAC supports a cursor function and three 256 by 8-bit color maps for its red, green, and blue video DACs. In addition, the Bt459 incorporates testability logic that allows the host to determine if the monitor is connected to the analog RGB outputs, and if the DACs are functional.

In order to avoid glitching of the video output, all Bt459 function updates should be performed during Vertical Sync times. Video interrupts are generated at the beginning of vertical retrace for this purpose. The Overlay Planes features of the Bt459 are not supported in hardware, and must be disabled by the sofware.

The Bt459 only supports byte reads and writes. Bt459 registers are word-aligned in the PMAG-BA Module’s address space. Reads or writes to the Bt459 complete at a rate of 7 cycles per byte.

Table 3-1 lists the Bt459 register addresses.

### Table 3-1: Bt459 Register Addresses

| Address | Register |
|---|---|
| 0xbb+2XXXX0 | Address Register Low Byte (AddrReg<7:0> |
| 0xbb+2XXXX4 | Address Register High Byte (AddrReg<15:8> |
| 0xbb+2XXXX8 | Register addressed by AddrReg<15:0> |
| 0xbb+2XXXXC | Color Map location addressed by AddrReg<15:0> |

Table 3-2 shows additional Bt459 registers and their indirect addresses.

### Table 3-2: Bt459 Indirectly Addressed Registers

| AddrReg<15:0> | R/W | Register | |
|---|---|---|---|
| 0000..00FF | ---- | Reserved | |
| 0100..010F | R/W | Overlay Color Reg 0..15 | (*) (**) |
| 0181..0183 | R/W | Cursor Color Reg 1..3 | (*) (**) |
| 0200 | R | ID Register (always reads as 4A) | |
| 0201 | R/W | Command Reg 0 (****) | |
| 0202 | R/W | Command Reg 1 | |
| 0203 | R/W | Command Reg 2 | |
| 0204 | R/W | Pixel Read Mask Register | |
| 0205 | ---- | Reserved | |
| 0206 | R/W | Pixel Blink Mask Register | |
| 0207 | ---- | Reserved | |
| 0208 | R/W | Overlay Read Mask Register | (*) |
| 0209 | R/W | Overlay Blink Mask Register | (*) |
| 020A | R/W | Interleave Register | (*) |
| 020B | R/W | Test Register | |
| 020C | R/W | Red Signature Register | |
| 020D | R/W | Green Signature Register | |
| 020E | R/W | Blue Signatuer Register | |
| 020F..02FF | ---- | Reserved | |
| 0300 | R/W | Cursor Command Register | |
| 0301 | R/W | Cursor (x) Low Register | |
| 0302 | R/W | Cursor (x) High Register | |
| 0303 | R/W | Cursor (y) Low Register | |
| 0304 | R/W | Cursor (y) High Register | |
| 0305 | R/W | Window (x) Low Register | |
| 0306 | R/W | Window (x) High Register | |
| 0307 | R/W | Window (y) Low Register | |
| 0308 | R/W | Window (y) High Register | |
| 0309 | R/W | Window Width Low Register | |
| 030A | R/W | Window Width High Register | |
| 030B | R/W | Window Height Low Register | |
| 030C | R/W | Window Height High Register | |
| 030D..03FF | ---- | Reserved | |
| 0400..07FF | R/W | Cursor RAM | |
| 0000..00FF | R/W | Color Map | (**) (***) |

( *) Not supported in Hwe

( **) Requires three read/write cycles (RGB)

(***) IO-Bus Addr must be 0xbb+2XXXXC

(****) After Command Reg 0 is initialized, a write to the ROM address space should be done to reset the video piplines.

### 3.2.1. Updating the Bt459 Color Map

To write the color map, load the Bt459's Address Register Low Byte with the desired Color Map entry address (00..FF), and then write the red, green, and blue values in three successive writes to the Color Map. Software must wait for the processor write buffers to flush after each Color Map write (the write buffers will overwrite data otherwise).

After the write of the blue color value (third data write), the Bt459 updates the color map with all 24 bits of color data, and increments the Addess Register Low Byte to the next map location. The same sequence may be repeated 256 times to fully update the color map. The Address Register will wrap only after it has been incremented to a count of 0FFF.

Reading the color map is similar to writing, except the host executes read cycles.

### 3.2.2. Updating Bt459 Control Registers

To access the Bt459 control registers, first load the Bt459's Address Register Low Byte and Address Register High Byte (AddrReg<15:0>) with the desired control register address, and then perform the read/write I/O cycle. After the control register write, the Bt459 will increment the Address Register in preparation for the next I/O cycle. Software must wait for the processor write buffers to flush after each register write (the write buffers will overwrite data otherwise). The Bt459's Address Register will wrap only after it has been incremented to a count of 0FFF.

Refer to the *Bt459 Functional Specification* in the Brooktree catalog for detailed programming instructions.

### 3.2.3. Screen Coordinates for the Bt459 Cursor

As outlined in the *Bt459 Functional Specification* , the (x,y) coordinate of the Bt459's cursor depends on hardware implementation. The equations that describe this dependency are:

Cx = desired display screen (x) position + H - P.

Cy = desired display screen (y) position + V - 32.

In the case of this video option (PMAG-BA), P = 52, H = 241, and V = 36 (decimal).

## 3.3. PMAG-BA Diagnostic ROM

The PMAG-BA Diagnostic ROM is located at 0xbb+380000 and at 0xbb+3C0000. The ROM is 64K-by 8-bits and is word-aligned. The data is presented on the least significant byte of the data bus. The most significant bytes will always read as FFFFFF. A write to this address space will return ready and generate a reset pulse to the video clock chip (Bt438). ROM reads will complete at a rate of 10 IO-Bus cycles per byte. The diagnostic ROM is in a socket.

## 3.4. Interrupts

### 3.4.1. General

Table 3-3 lists the I/O device connections to the R3000 interrupt inputs. The state of the interrupt signals is continually reflected in the R3000 CAUSE register at the bit position shown in the table. Note that a given interrupt signal only generates an R3000 exception if it is enabled in the STATUS register interrupt mask field, and interrupts are enabled by the STATUS<0> register bit. Note also that the interrupt signals are visible in the CAUSE register regardless of the state of the STATUS interrupt mask. That is, the operating system interrupt dispatcher must explicitly check that a given interrupt level, which is asserted in the CAUSE register, is enabled before activating that interrupt level's handler.

**Table 3-3: I/O Interrupt Levels**

| Level | CAUSE/STATUS | I/O Device |
|---|---|---|
| 5 | 15 | FPU |
| 4 | 14 | Reserved |
| 3 | 13 | Memory Error |
| 2 | 12 | Reserved |
| 1 | 11 | Real Time Clock |
| 0 | 10 | Local |

Due to the increased number of I/O devices supported in DS5000 systems, all I/O interrupts are merged into a single R3000 interrupt. However, the individual I/O device interrupts are visible through the system module interrupt status register. The bits in the register are as shown in the Table 3-4

**Table 3-4: Local Interrupt Status Register**

| Bit | I/O Device |
|---|---|
| 7 | Serial Lines |
| 6 | System module embedded I/O slot 6 |
| 5 | System module embedded I/O slot 5 |
| 4 | Reserved |
| 3 | Reserved |
| 2 | Option Connector 2 |
| 1 | Option Connector 1 |
| 0 | Option Connector 0 |

The PMAG-BA Module will interrupt the CPU through the Local interrupt at level 0, which will be visible on the R3000 CAUSE<10> register bit. The host should then read the Local Interrupt Status register to determine which I/O device is interrupting. The bits in the Interrupt Status register are cleared automatically when the interrupt line of the respective device is cleared by the software.

### 3.4.2. Video Interrupts

After power-up, and at the end of every frame hence, the PMAG-BA Module will generate video interrupts. Video interrupts (option interrupts) can be disabled by writing the "IOINTEN" control bits in the system module's control and status register (CSR). There is no mechanism on the PMAG-BA Module to permanently disable video interrupts. In order to clear video interrupts, the host must write the PMAG-BA Module's IReq Control Address (value written is don't care). It is recommended that the software first clear the video interrupt and then enable option interrupts. This will insure that stale video interrupts are removed and will synchronize the next video interrupt to the end of the next frame. From the time the video interrupt initially asserts, until the first pixel of the next frame is displayed is 37 scan lines (approximately 688 microseconds).

## 3.5. Video Timing

Table 3-5 shows the PMAG-BA video timing.

### Table 3-5: Video Timing

| | | | |
|---|---|---|---|
| **Horizontal Timing** | | | |
| | Pixel Clock | 69.1968 MHz | 14.45 ns |
| | Active Video | 1024 pixels | 14.796 us |
| | Blanking | 256 pixels | 3.699 us |
| | Total Line | 1280 pixels | 18.496 us |
| | Sync Front Porch | 12 pixels | 173.4 ns |
| | Sync Width | 128 pixels | 1.849 us |
| | Sync Back Porch | 116 pixels | 1.676 us |
| **Vertical Timing** | | | |
| | Line Rate | 54.062 KHz | 18.496 us |
| | Active Video | 864 lines | 15.98 ms |
| | Blanking | 37 lines + 256 pixels | 688.051 us |
| | Total Lines | 901 lines | 16.664 ms |
| | Sync Front Porch | 12 pixels | 173.4 ns |
| | Sync Width | 3 lines | 55.488 us |
| | Sync Back Porch | 34 lines + 244 pixels | 632.389 us |
| **Video Levels** | | | |
| | Impedance | 75 Ohms, Double Termination | |
| | Sync Level (Green) | 0.000 V | |
| | Blank Level (Red, Blue) | 0.000 V | |
| | Blank Level (Green) | 0.286 V | |
| | Black Level (Red, Blue) | 0.054 V | |
| | Black Level (Green) | 0.340 V | |
| | White Level (Red, Blue) | 0.714 V | |
| | White Level (Green) | 1.000 V | |